Ultra Low-Power Receiver Design for Dense Optical Interconnects

Meisam Honarvar Nazari, Azita Emami-Neyestanak
California Institute of Technology, Pasadena, CA

With the increasing bandwidth requirements of computing systems and limitations on power consumption, optical signaling for chip-to-chip interconnects has gained a lot of interest. Hybrid integration of optical devices with electronics has been demonstrated to achieve high performance [1]-[4], and recent advances in silicon photonics have led to fully integrated systems [5]. These approaches pave the way to massively parallel optical communications. Dense arrays of optical detectors require very low-power, sensitive, and compact optical receiver circuits. Existing designs for the input receiver, such as TIA, require large power consumption to achieve high bandwidth and low noise, and can occupy large area due to bandwidth enhancement inductors. In this work, a compact low-power optical receiver that scales well with technology has been designed to explore the potential of optical signaling for future chip-to-chip and on-chip communication. In most optical receivers, the photodiode current is converted to a voltage signal. A simple resistor can perform the I-V conversion if the resulting RC time constant is in the order of the bit interval (T_b) [5]. However, for a given photodiode capacitance and target SNR, the RC limits the bandwidth and hence the data rate. To avoid this problem, TIAs are commonly employed, which are highly analog, power hungry, and do not scale well with technology. One alternative is the integrating front-end to eliminate the need for resistance and breaking the bandwidth trade-off. However, this technique suffers from voltage headroom limitations, and requires short-length DC-balanced inputs [6]. The proposed receiver resolves this problem by employing an integrating RC front-end along with dynamic offset modulation technique that decouple the bandwidth/data-rate and integration/headroom trade-offs [7].

Fig. 1 shows the top-level architecture of the receiver. The input current from the photodiode is integrated over the parasitic capacitor, while the shunt resistor (R_s) limits the voltage. R_s and C_{PD} create a time constant that is much larger than T_b ($RC>>T_b$). The resulting voltage at the input is sampled every bit interval to determine whether a zero or one has been received. This process is performed by comparing the two consecutive samples, as shown in Fig. 1, however, due to the RC nature of the front-end, after several consecutive ones or zeros, the voltage reaches to the saturation level and results in close to zero voltage difference at the input of the sense amplifier, as shown in Fig. 3. This dependency on input can be resolved by introducing a dynamic offset to the sense amplifier based on the value of the input voltage. This offset effectively increases the voltage difference ΔV_{amp} for weak ones/zeros, Fig. 3.

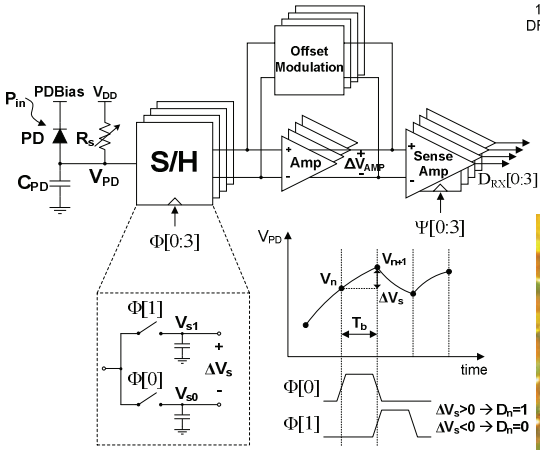


Fig. 1. Receiver top-level architecture.

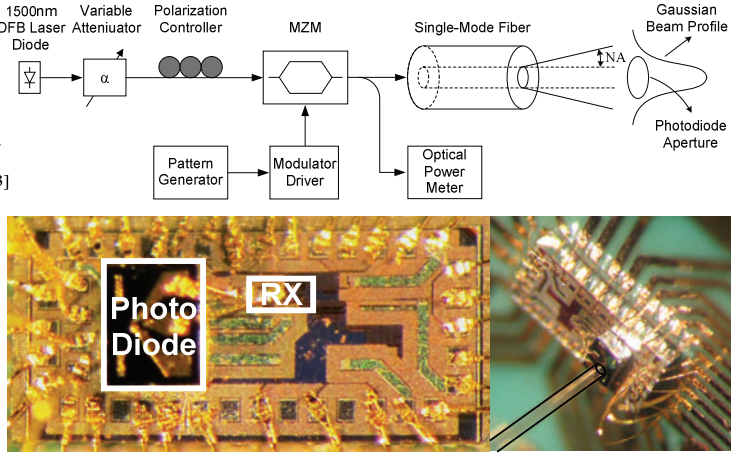


Fig. 2. Optical test set-up, micrograph of the receiver with bonded photodiode.

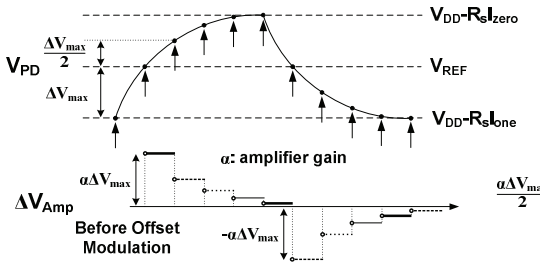
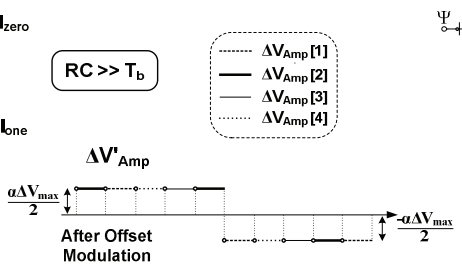


Fig. 3. Dynamic offset modulation technique.



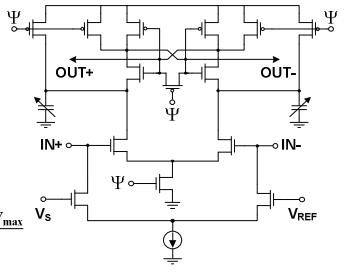


Fig. 4. Sense amplifier.

In this technique, the introduced offset is proportional to the difference between the sampled voltage and V_{REF} with a proportionality coefficient denoted as β. It can be shown mathematically that for an exponential decaying signal, β can be chosen such that $\Delta V'_{amp}$ is always equal to $\Delta V_{max}/2$, where ΔV_{max} is the maximum voltage difference and it occurs for a transition after many consecutive ones or zeros. As a result, a constant voltage difference can be guaranteed at the input of the sense amplifier, regardless of the received input pattern. Similar to [6], the employed double-sampling technique allows demultiplexing by use of multiple clock phases and samplers. Fig. 4 shows the sense amplifier employed in this design. The dynamic offset is introduced through the bottom differential pair.

The prototype was fabricated in a 65nm CMOS technology and occupies less than 0.0028mm^2, Fig. 2. The receiver was wire-bonded to a high speed photodiode and tested at different data rates. The total capacitance at the receiver input was estimated to be more than 200fF. Fig. 2 shows the optical test setup. The optical beam from a DFB laser diode is modulated by a high speed Mach-Zender modulator and coupled to the photodiode through a single-mode fiber. The total free space coupling loss from the fiber tip to the photodiode is estimated to be about 3-4dB. Fig. 5 shows how the sensitivity of the receiver for BER<10^{-12} changes with data rate. Note that the coupling loss is not considered in this plot, and the sensitivity will improve considerably if the coupling is optimized. The receiver achieves more than -12.5dBm of sensitivity at 10Gb/s that reduces to -4.6dBm at 24Gb/s. The receiver power consumption at different data rates is also shown in Fig. 6. The power increases linearly with the data rate as the receiver employs mostly digital blocks. The receiver offers a peak power efficiency of 0.36mW/Gb/s at 20Gb/s data rate. Employing mainly digital blocks in this design facilitates the migration process to more advance technology nodes. The power consumption and speed of the receiver scale well with the scaling of CMOS technology. For instance, simulation results show that at given data rate, a factor of four reduction in power consumption can be achieved by scaling the proposed design to 28nm CMOS technology node.

Silicon photonics has offered high-performance optical components, such as Germanium photodiodes, waveguides and modulators, alongside transistors. This integration allows for very small photodiode parasitic capacitance. Fig. 7 shows how the receiver current sensitivity (for BER<10^{-12}) changes with scaling the photodiode capacitance (solid and dashed curves). By essence, due to integrating nature of the receiver, the RX sensitivity must linearly increase by lowering the photodiode capacitance (solid curve). However, as a result of charge sharing between the photodiode and sampling capacitances, a certain ratio (about 10%) between their sizes has to be kept to minimize error. Since scaling of the sampling capacitance increases the noise, for a target SNR, a larger current is required, as shown in Fig. 7 (dashed curve). For the target RX sensitivity, this figure also shows how the data rate changes as the photodiode capacitance scales (dotted curve). The maximum achievable data rate is ultimately limited by the speed of transistors, which in 65nm technology node is about 40-50Gb/s.

The proposed optical receiver provides high power efficiency and data rate. The novel architecture is well-suited for future integrated highly-scaled CMOS and silicon photonics technologies. Experimental results validate the feasibility of the receiver for ultra-low-power, high-data rate and highly parallel optical links.

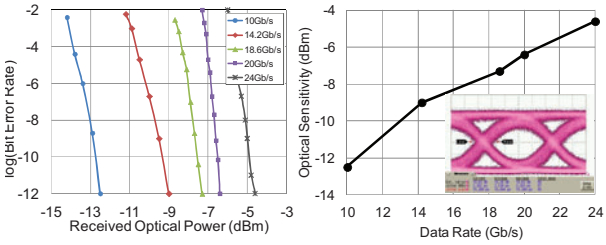


Fig. 5. Receiver optical power sensitivity at different data rates.

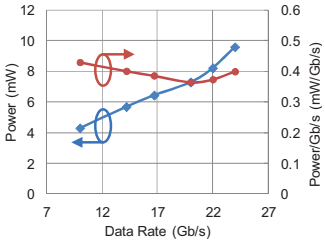


Fig. 6. Receiver power efficiency.

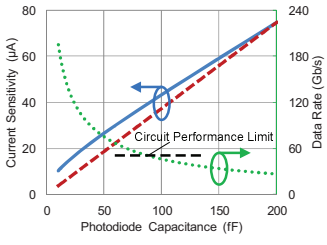


Fig. 7. RX Sensitivity and data rate vs photodiode capacitance.

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